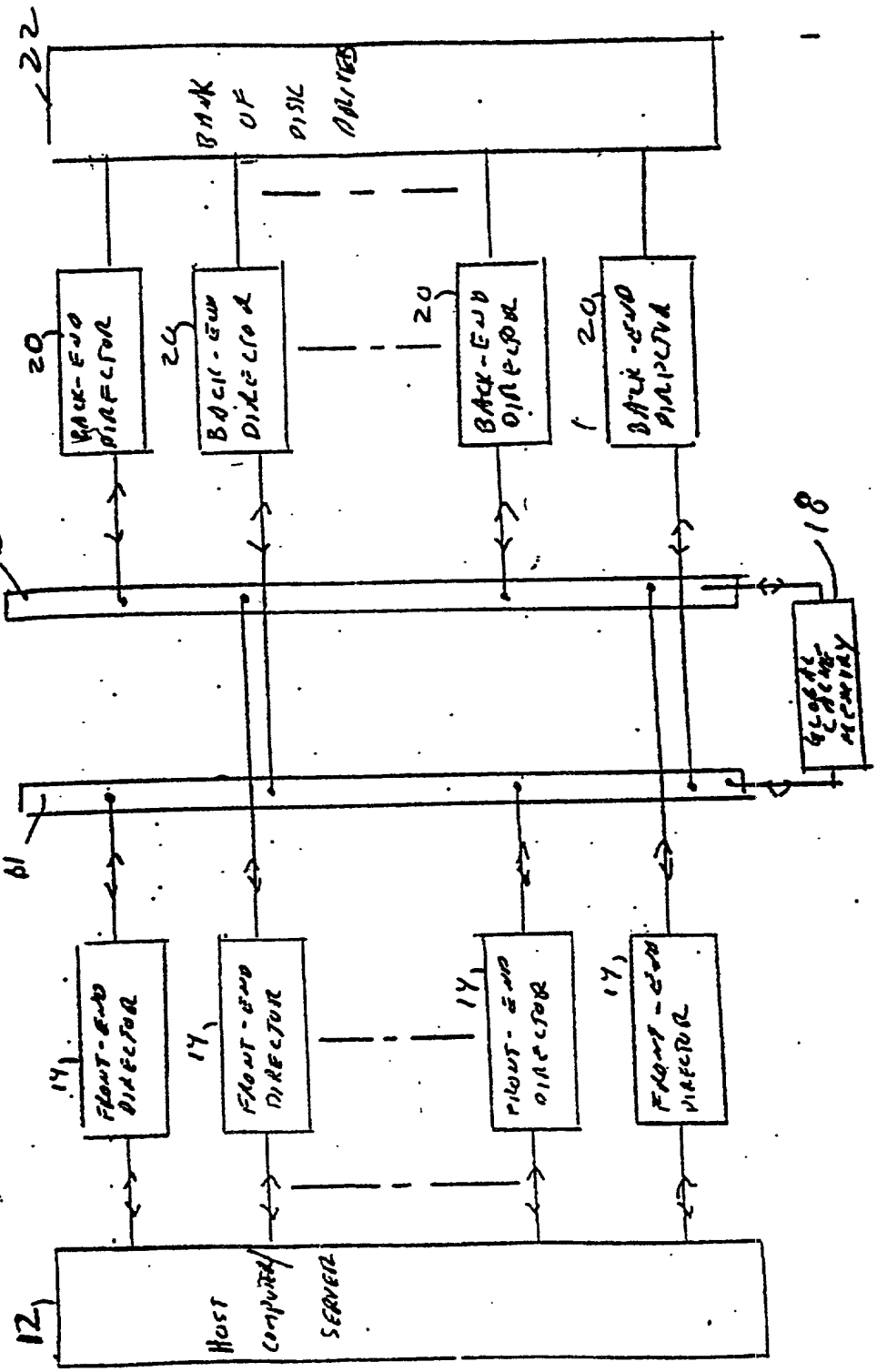


FIG. 1
PRIOR ART

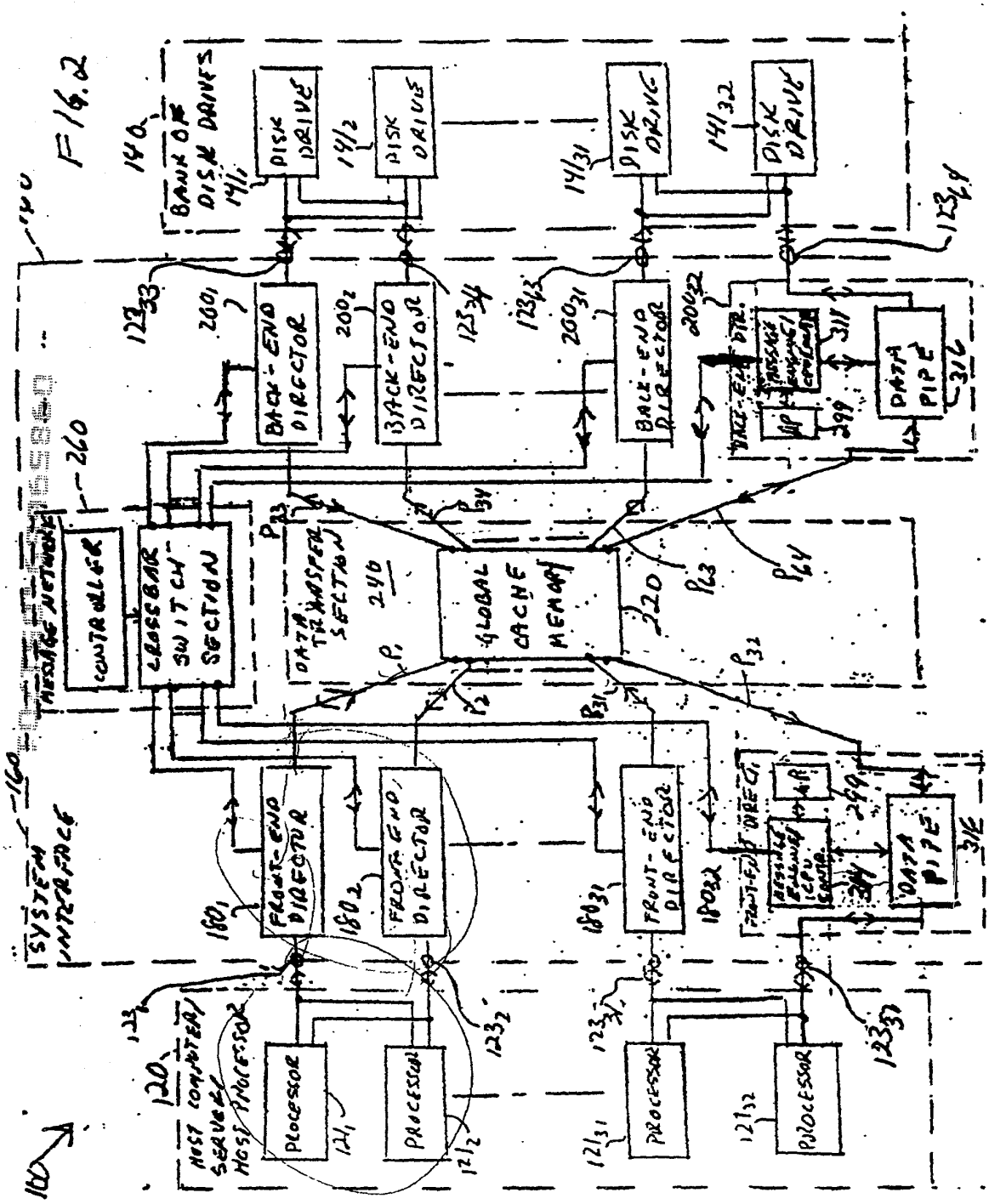


FIG. 2
100
120
HOST COMPUTER/ SERVER/ HOST PROCESSOR
121
PROCESSOR
123
140
BANK OF DISK DRIVES
141
DISK DRIVE
160
SYSTEM INTERFACE
180
FRONT-END DIRECTOR
200
BACK-END DIRECTOR
240
DATA TRANSFER SECTION
220
GLOBAL CACHE MEMORY
260
MESSAGE NETWORK
CONTROLLER
CROSSBAR SWITCH SECTION
300
DATA PIPE

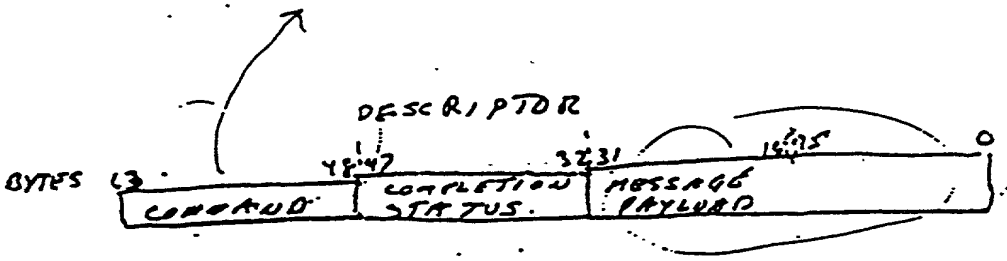

DESCRIPTOR
BYTES
63
48:47
32:31
15:15
0
COMMAND
COMPLETION STATUS
MESSAGE PAYLOAD

FIG 2A

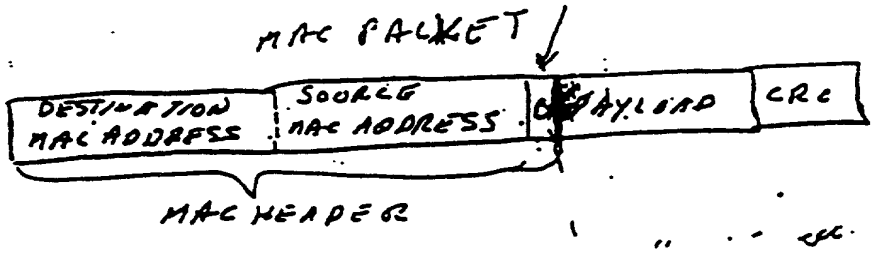

MAC PACKET
DESTINATION MAC ADDRESS
SOURCE MAC ADDRESS
PAYLOAD
CRC
MAC HEADER

FIG 2B

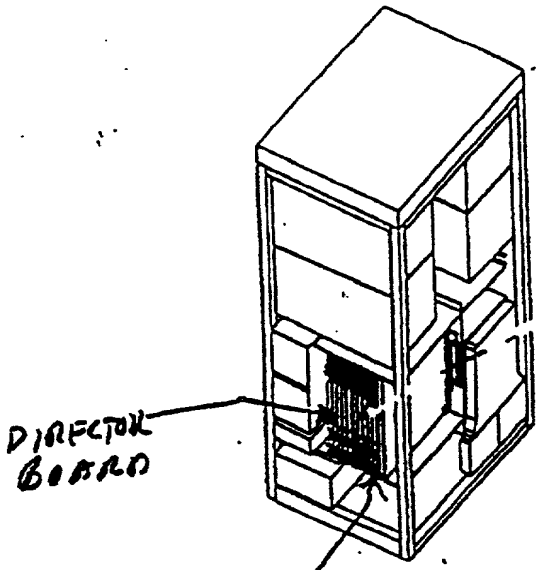
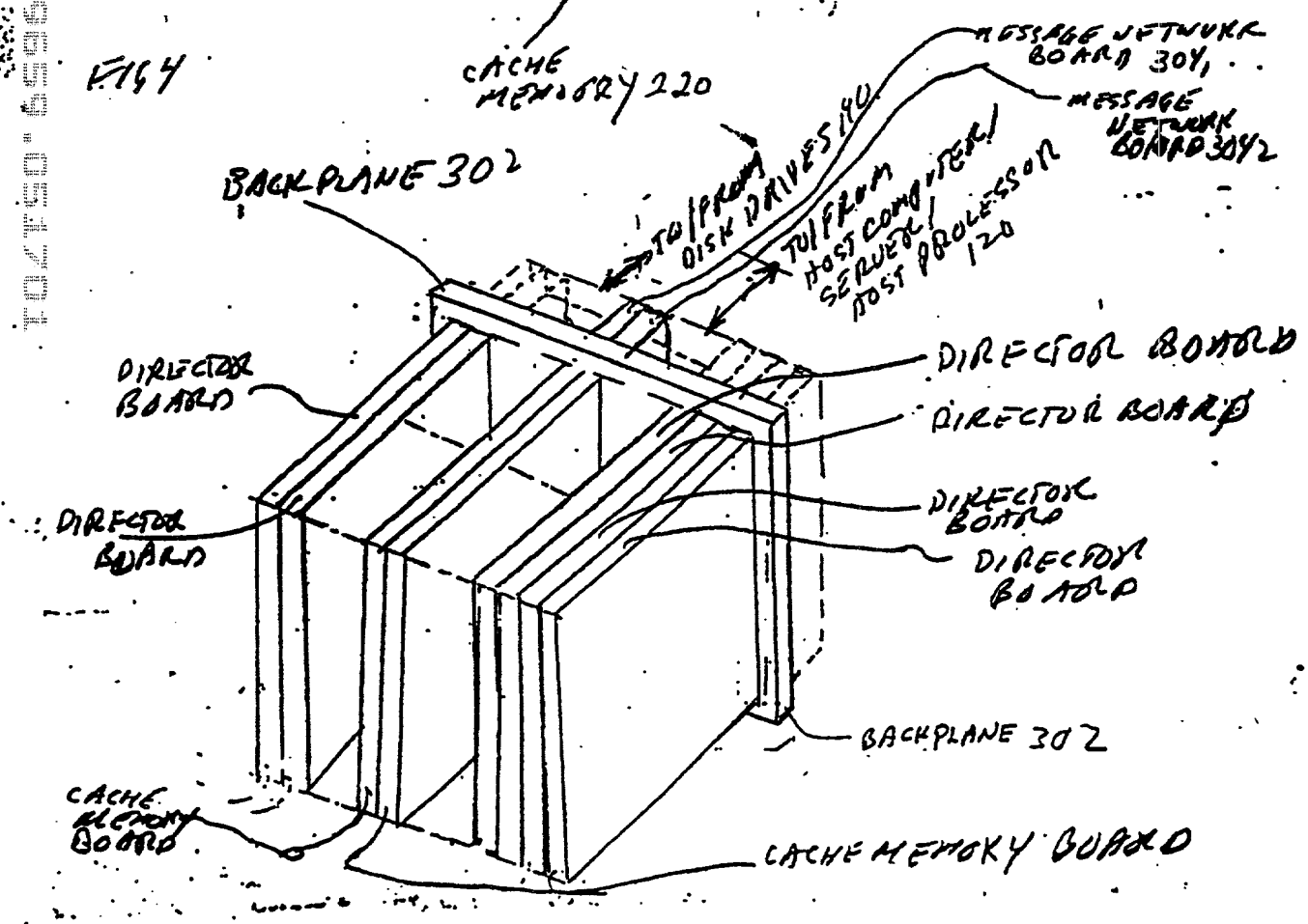

DIRECTOR
BOARD
CACHE
MEMORY 220

FIG. 3

FIG 4


MESSAGE NETWORK
BOARD 304,
MESSAGE
NETWORK
BOARD 304,2
BACKPLANE 302
TO/FROM
DISK DRIVES 140
TO/FROM
HOST COMPUTER/
HOST PROCESSOR
120
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR
BOARD
DIRECTOR
BOARD
DIRECTOR
BOARD
DIRECTOR
BOARD
BACKPLANE 302
CACHE
MEMORY
BOARD
CACHE MEMORY BOARD

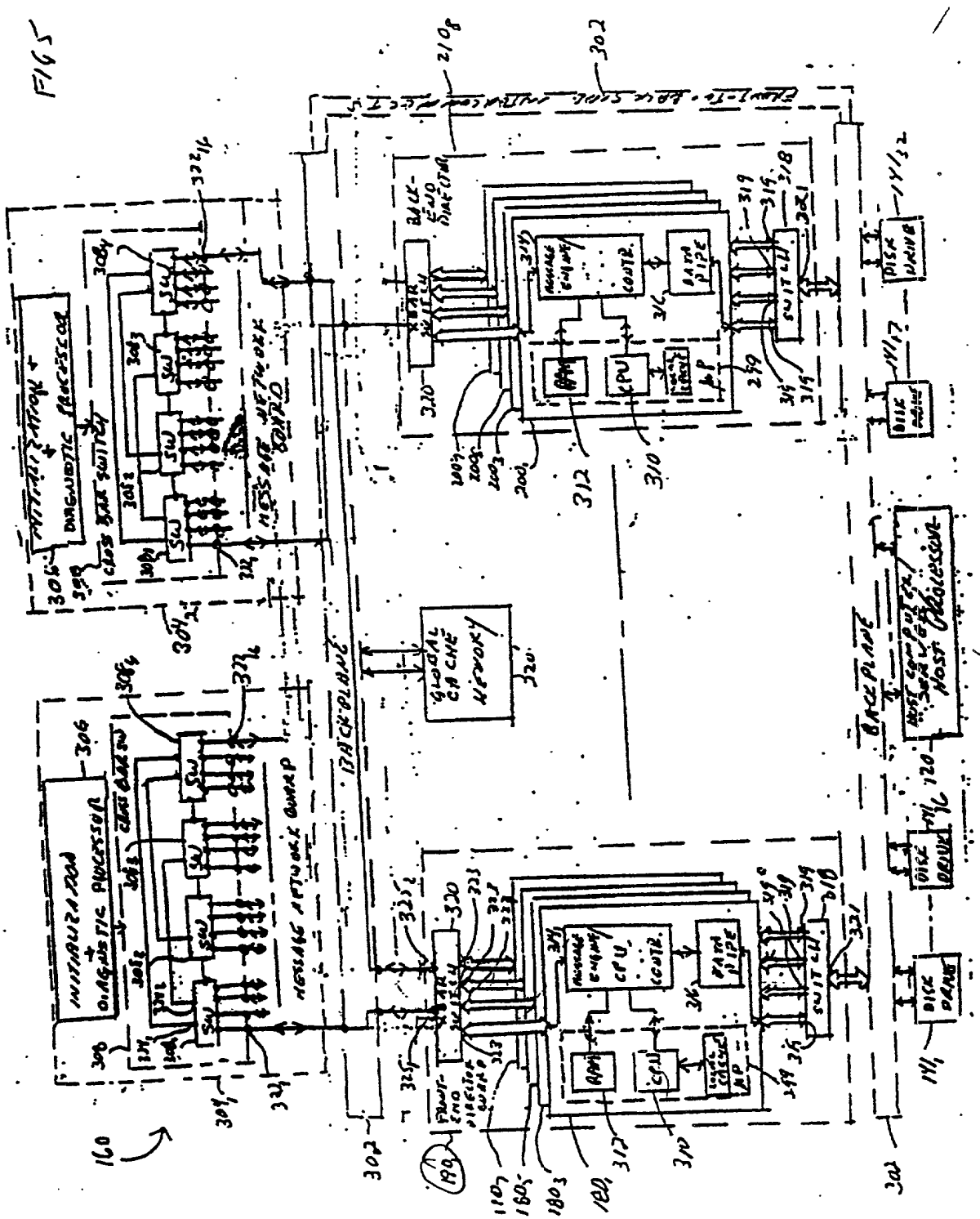
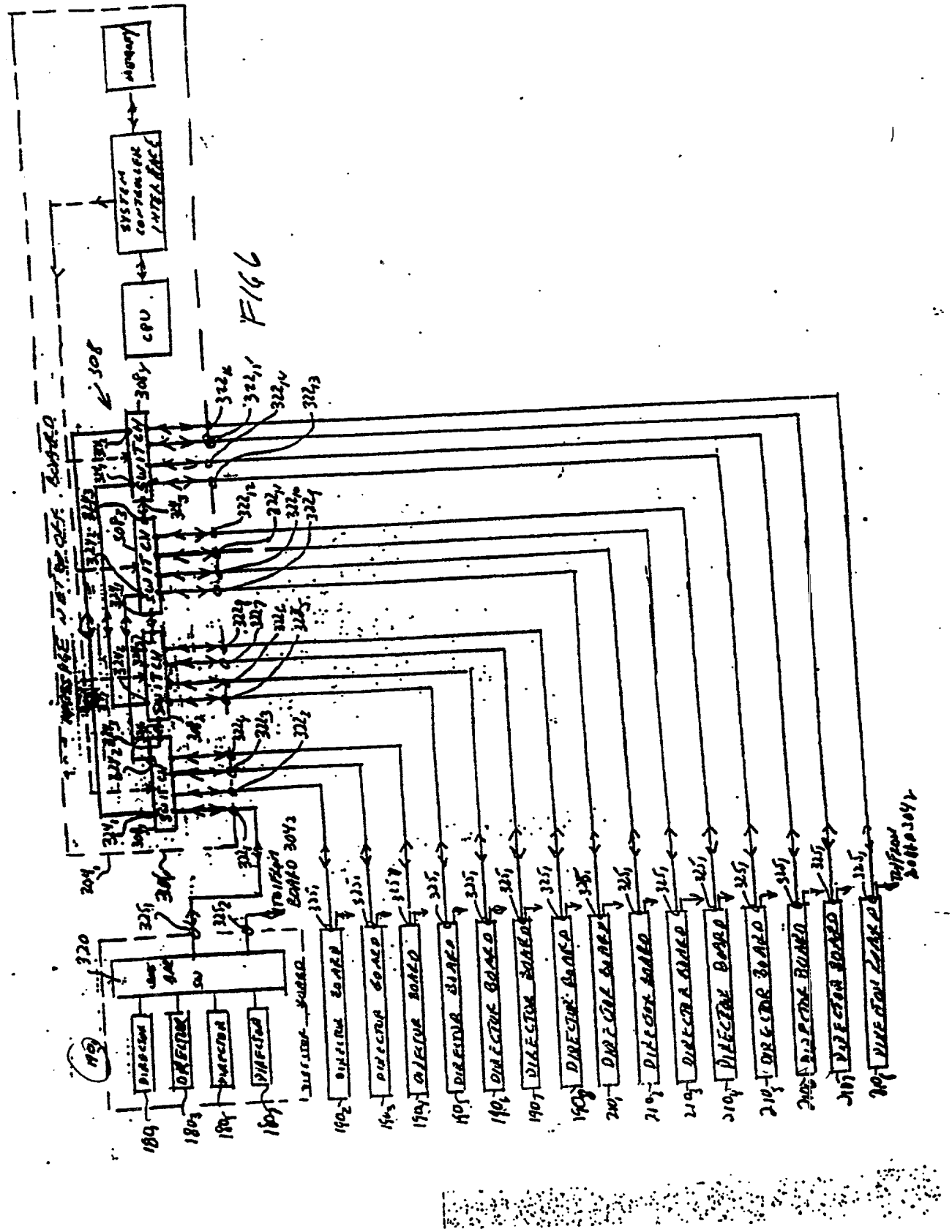
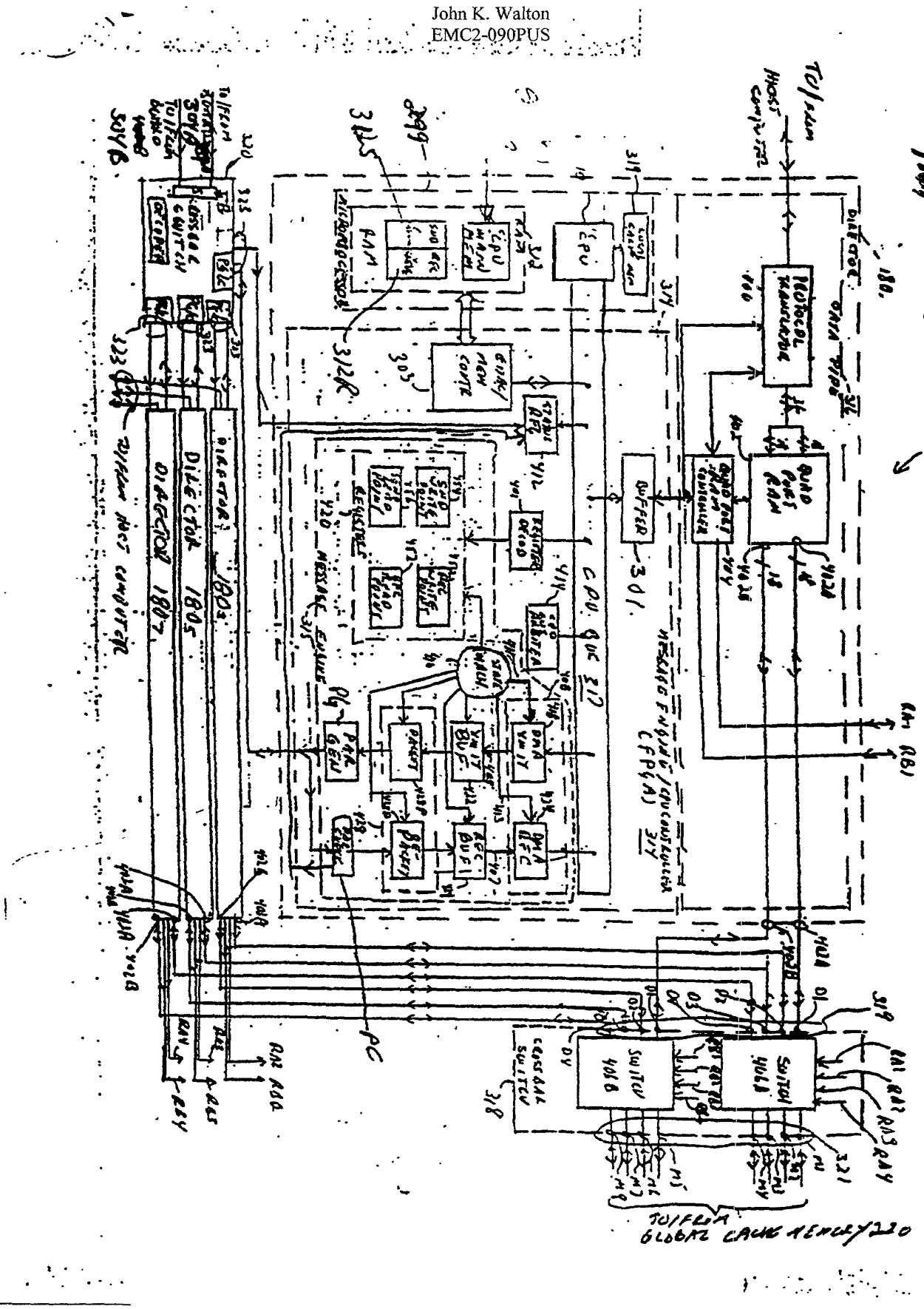


FIG 5
160
302
304
306
308
310
312
314
316
318
320
322
324
326
328
330
332
334
336
338
340
342
344
346
348
350
352
354
356
358
360
362
364
366
368
370
372
374
376
378
380


CPU
SYSTEM CONTROLLER INTERFACE
MEMORY
DIRECTOR
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD



09858585 052701

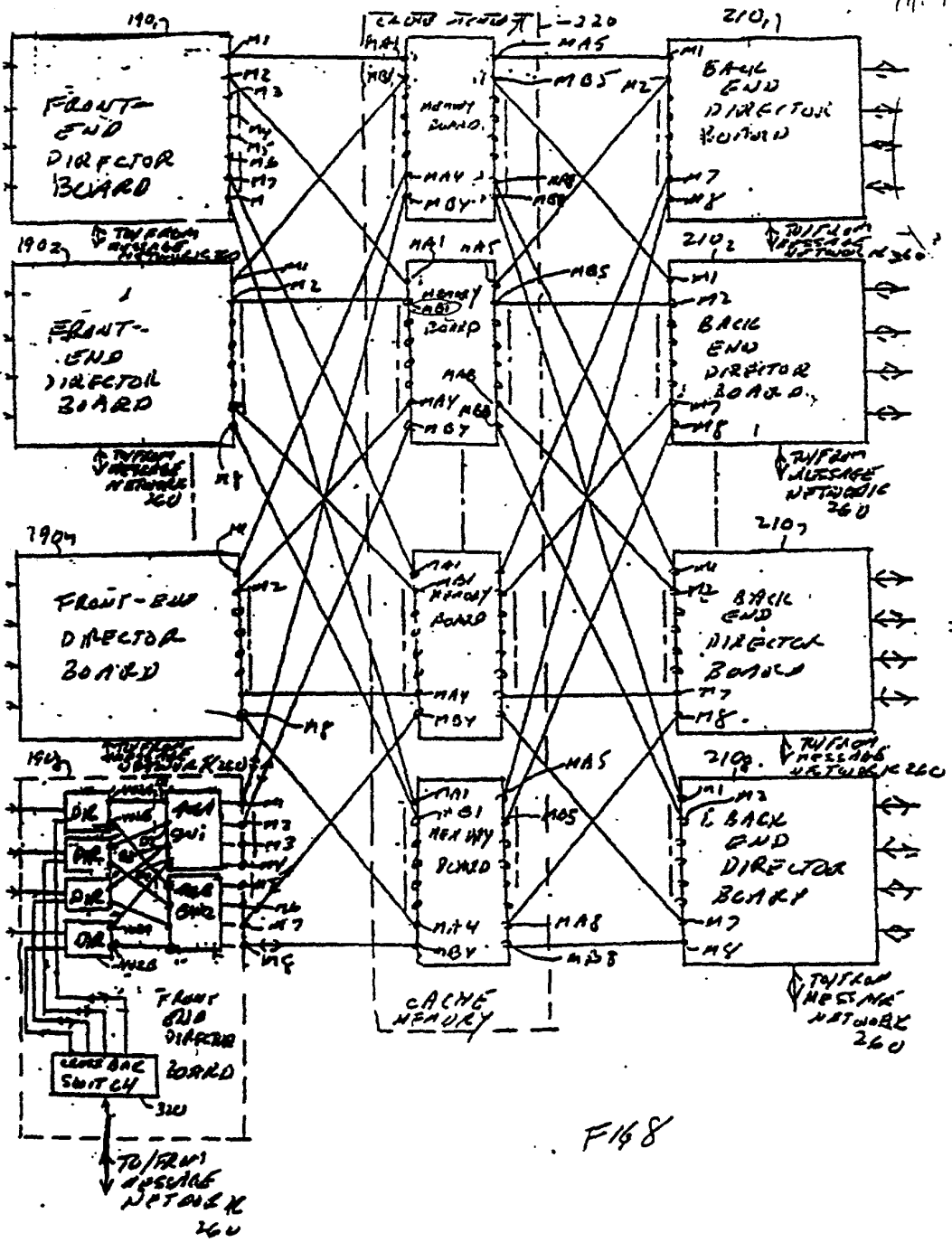

FRONT-END DIRECTOR BOARD
BACK END DIRECTOR BOARD
CACHE MEMORY
TO/FROM MESSAGE NETWORK 260
FRONT END DIRECTOR BOARD
SERVICE SWITCH
310
TO/FROM MESSAGE NETWORK 260

FIG 8

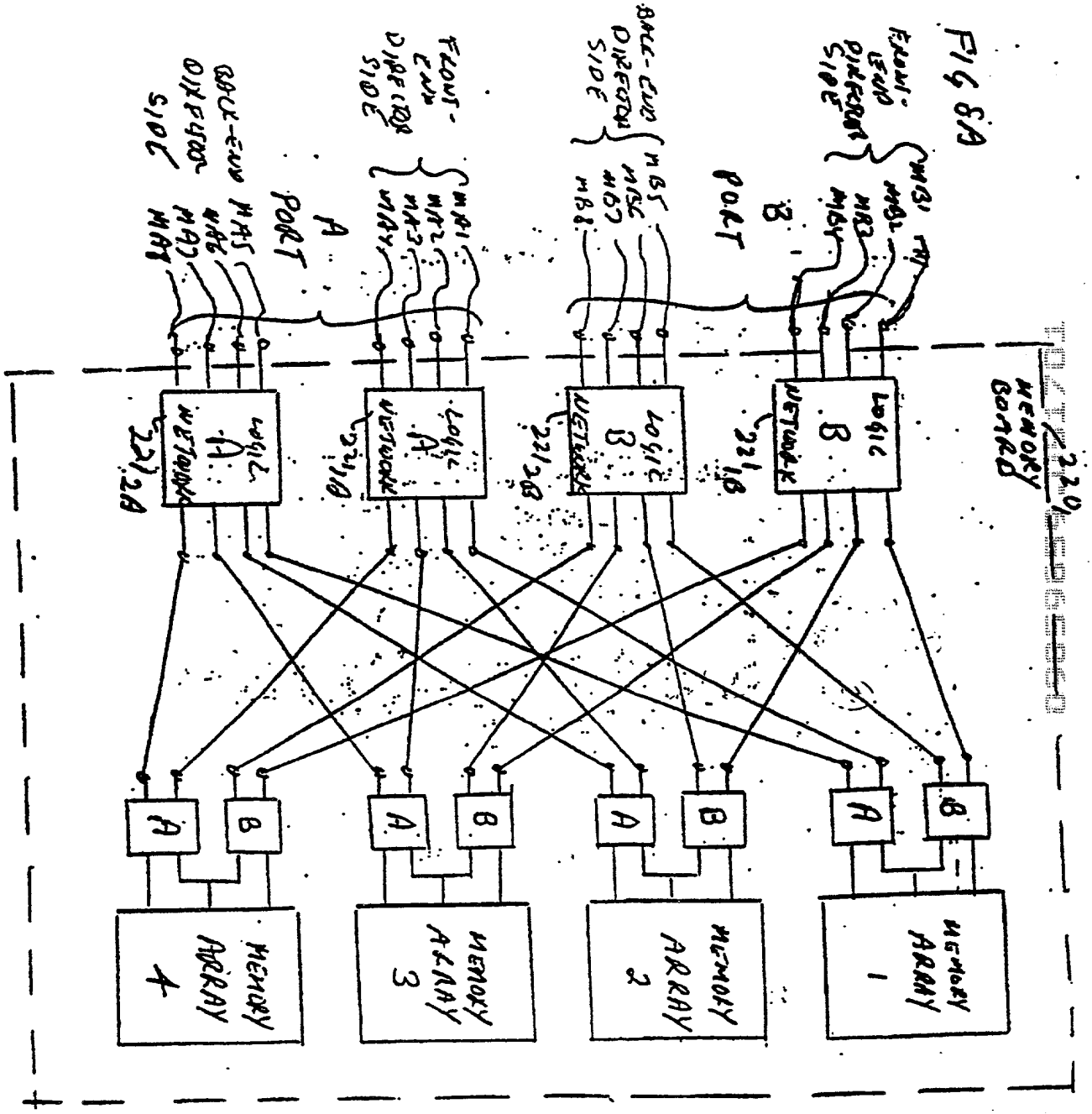


FIG 8A
MEMORY BOARD
220
FRONT-END DIRECTOR SIDE
MB3
MB2
MB1
MB0
B PORT
BACK-END DIRECTOR SIDE
MB5
MB4
MB3
FRONT-END DIRECTOR SIDE
MA1
MA2
MA3
MA4
A PORT
BACK-END DIRECTOR SIDE
MA5
MA6
MA7
MA8
LOGIC B NETWORK
221B
LOGIC A NETWORK
221A
A
B
MEMORY ARRAY 1
MEMORY ARRAY 2
MEMORY ARRAY 3
MEMORY ARRAY 4

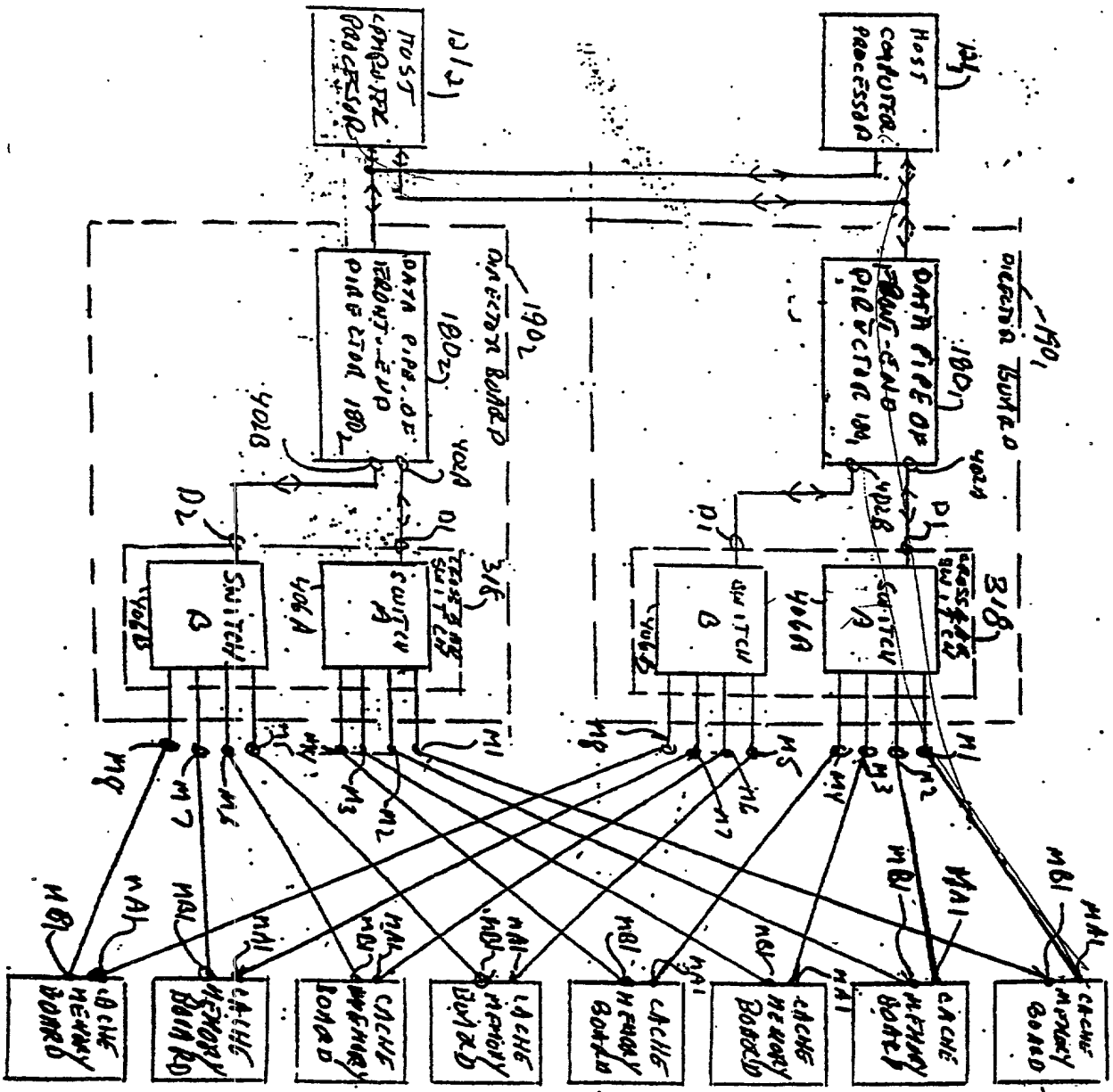
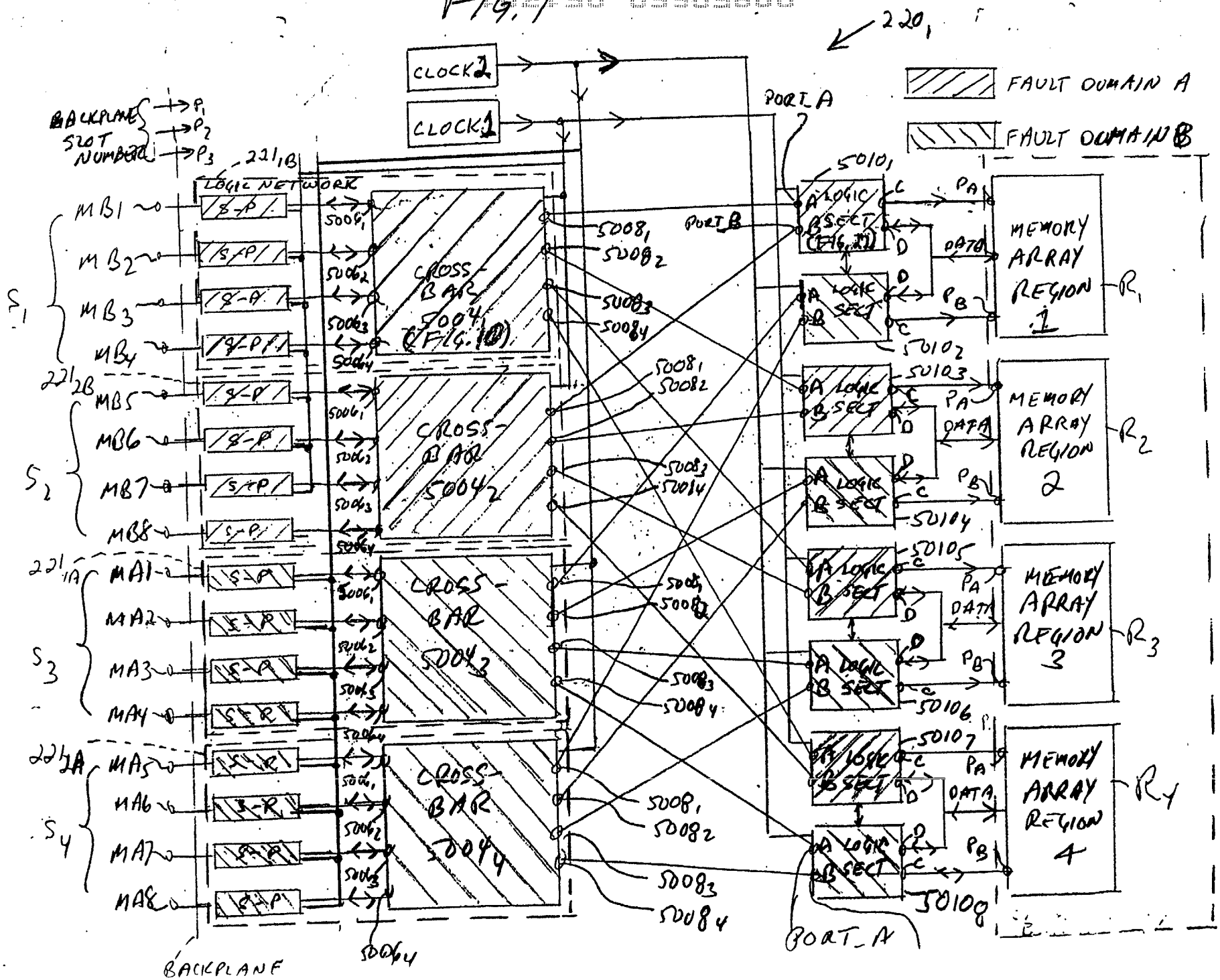

HOST COMPUTER PROCESSOR
DATA PIPE OR BUS-EXTENDER
SWITCH A
SWITCH B
CACHE MEMORY BOARD
CACHE MEMORY BOARD
CACHE MEMORY BOARD
CACHE MEMORY BOARD
CACHE MEMORY BOARD
CACHE MEMORY BOARD
CACHE MEMORY BOARD
CACHE MEMORY BOARD

FIG 8B

Data Storage System Having No-Operation Command
John K. Walton
EMC2-090PUS

FIG. 9



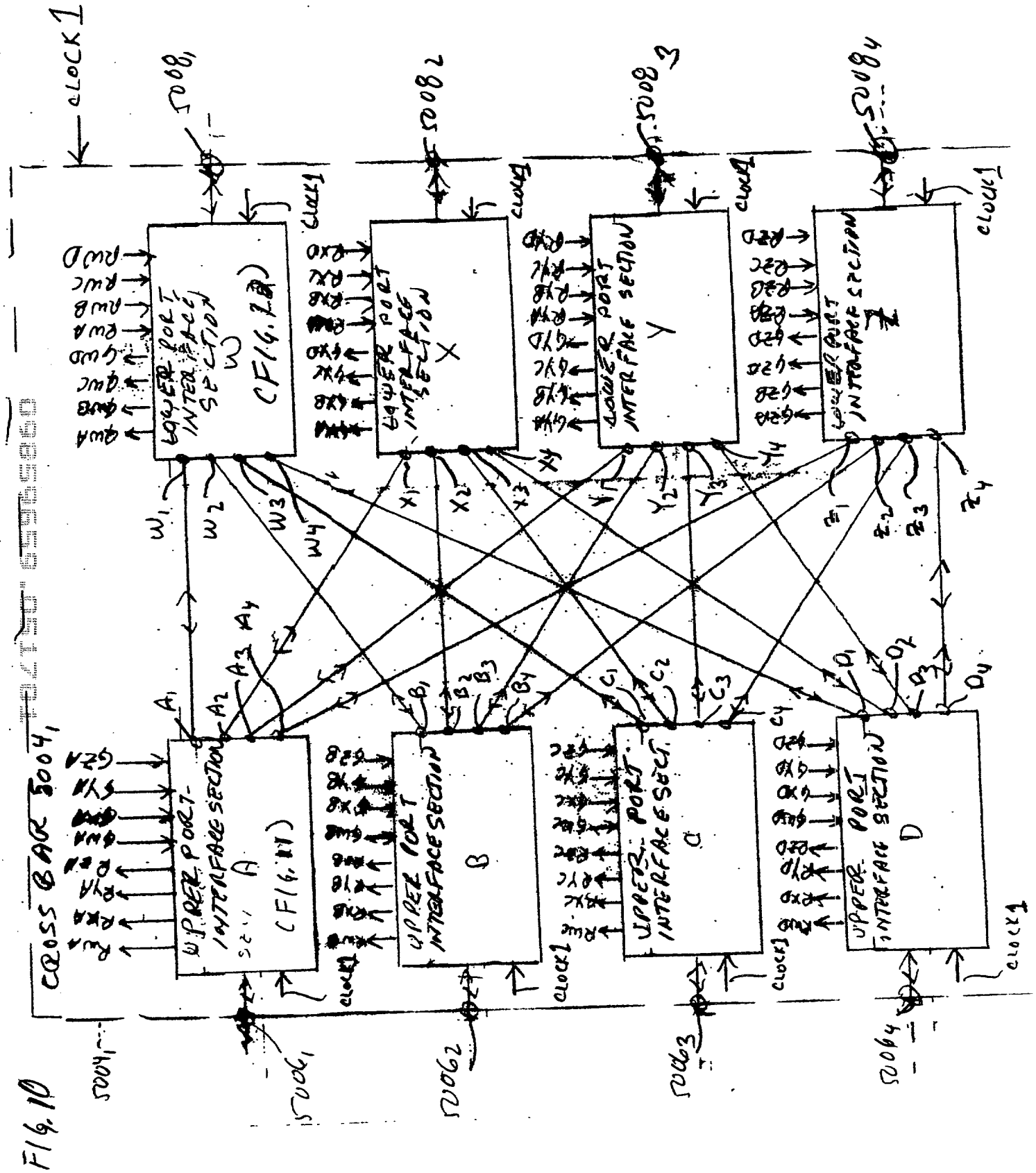
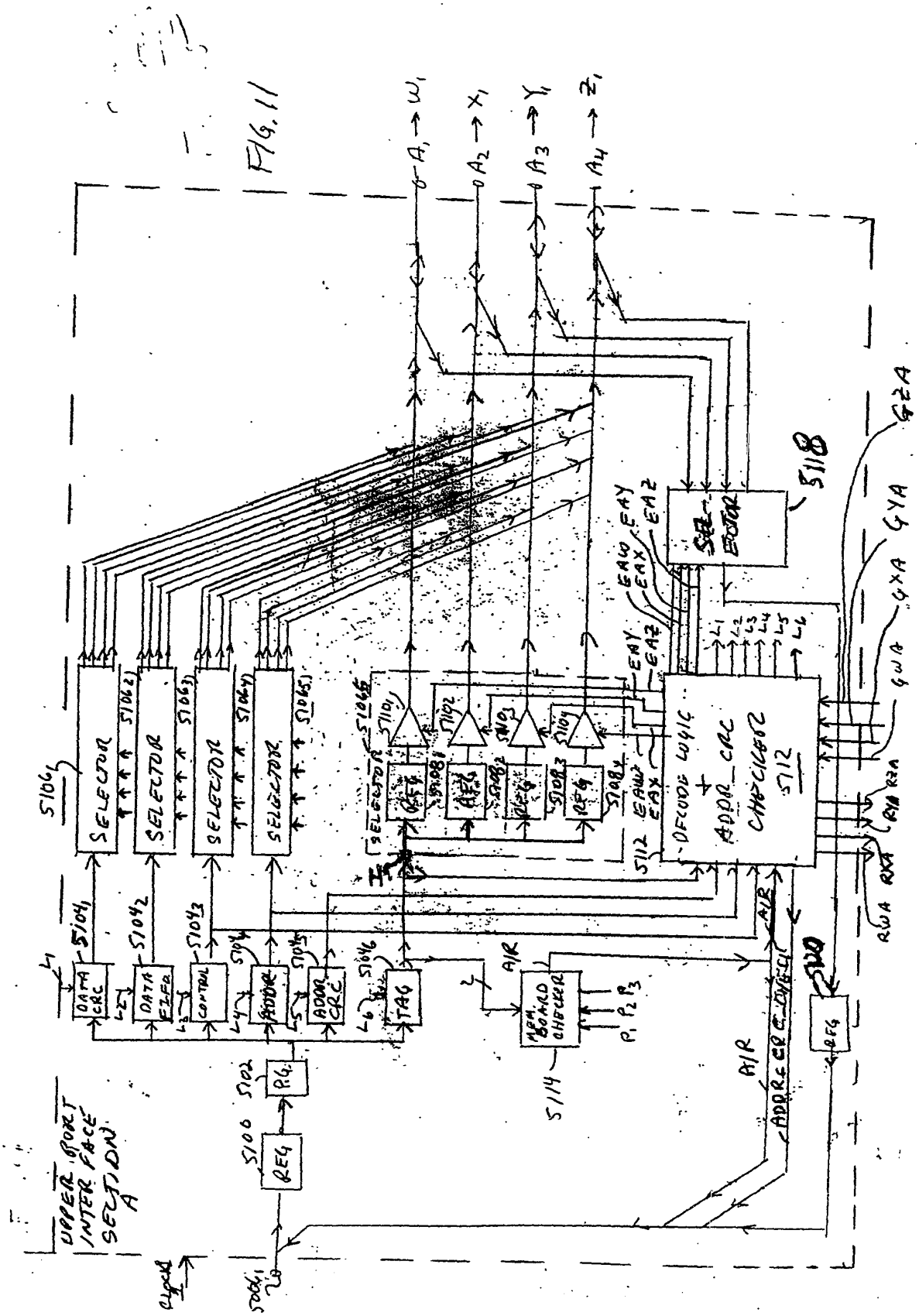

CROSS BAR 500
CLOCK 1
LOWER PORT INTERFACE SECTION W
LOWER PORT INTERFACE SECTION X
LOWER PORT INTERFACE SECTION Y
LOWER PORT INTERFACE SECTION Z
UPPER PORT INTERFACE SECTION A
UPPER PORT INTERFACE SECTION B
UPPER PORT INTERFACE SECTION C
UPPER PORT INTERFACE SECTION D
CLOCK 1

FIG. 10



09595959.051705

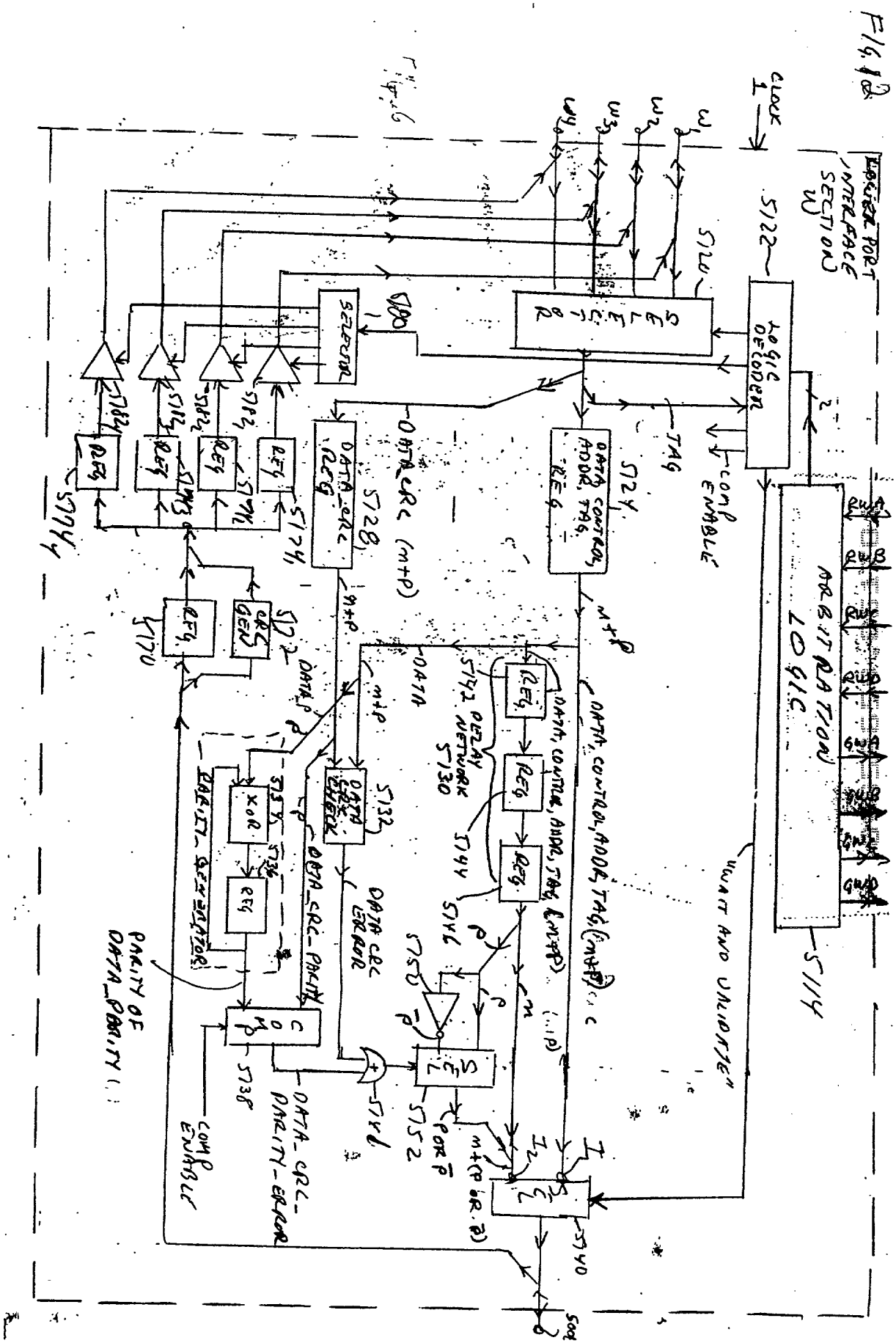


FIG. 1B
CLOCK 1
5122
5124
SELECTOR
LOGIC DECODER
TAG
COMP ENABLE
5126
DATA CONTROL, ADDR, TAG, (m+p) REG
5128
DATA_CRC (m+p)
DATA_CRC GEN
5130
DELAY NETWORK
5132
DATA CRC ERROR
5134
XOR
5136
REG
5138
COMP ENABLE
PARITY OF DATA_PARITY
DATA_CRC_PARITY
DATA_CRC_PARITY-ERROR
5140
5142
5144
5146
5148
5150
5152
5154
5156
5158
5160
5162
5164
5166
5168
5170
5172
5174
5176
5178
5180
5182
5184
5186
5188
5190
5192
5194
5196
5198
5200
5202
5204
5206
5208
5210
5212
5214
5216
5218

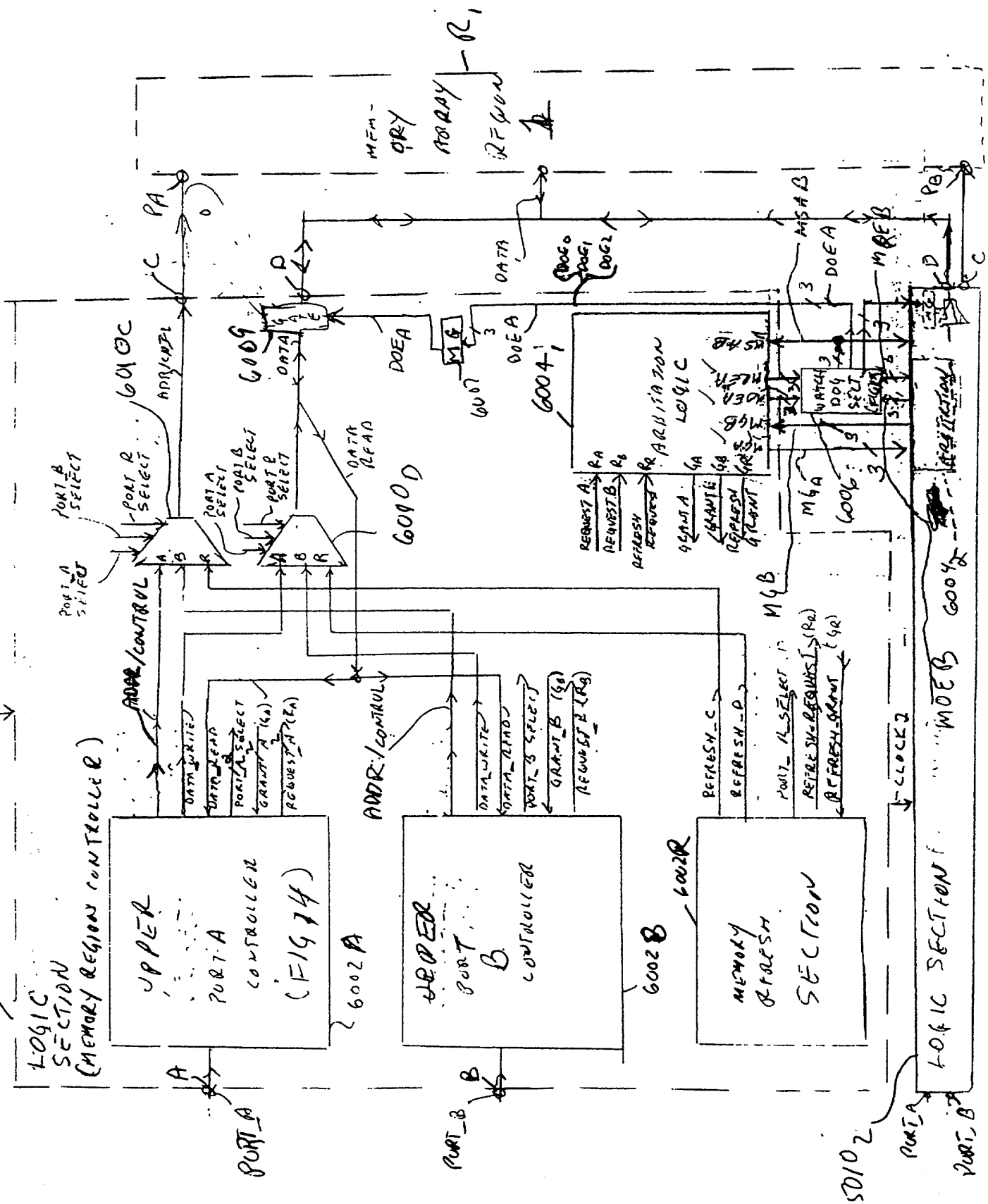
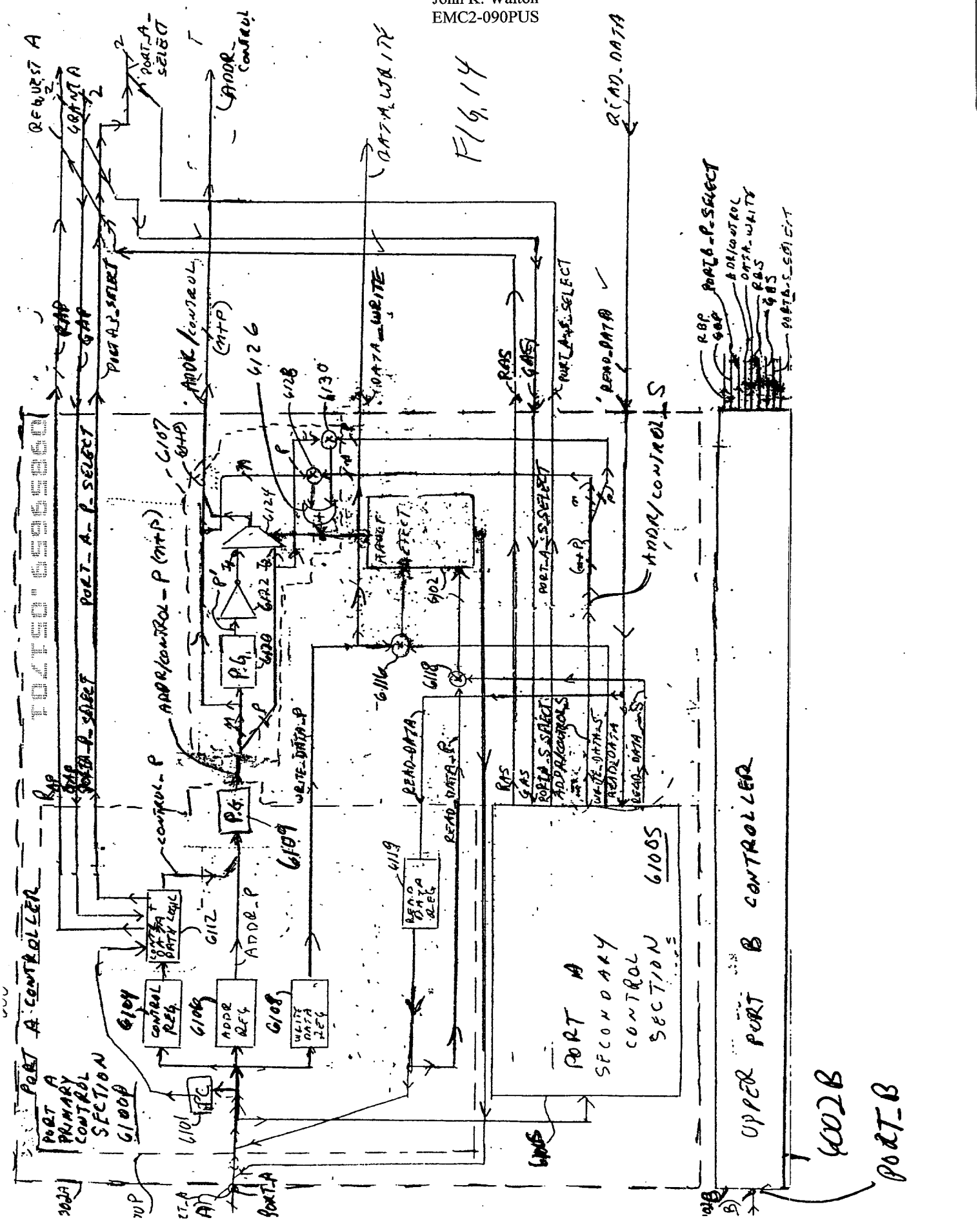
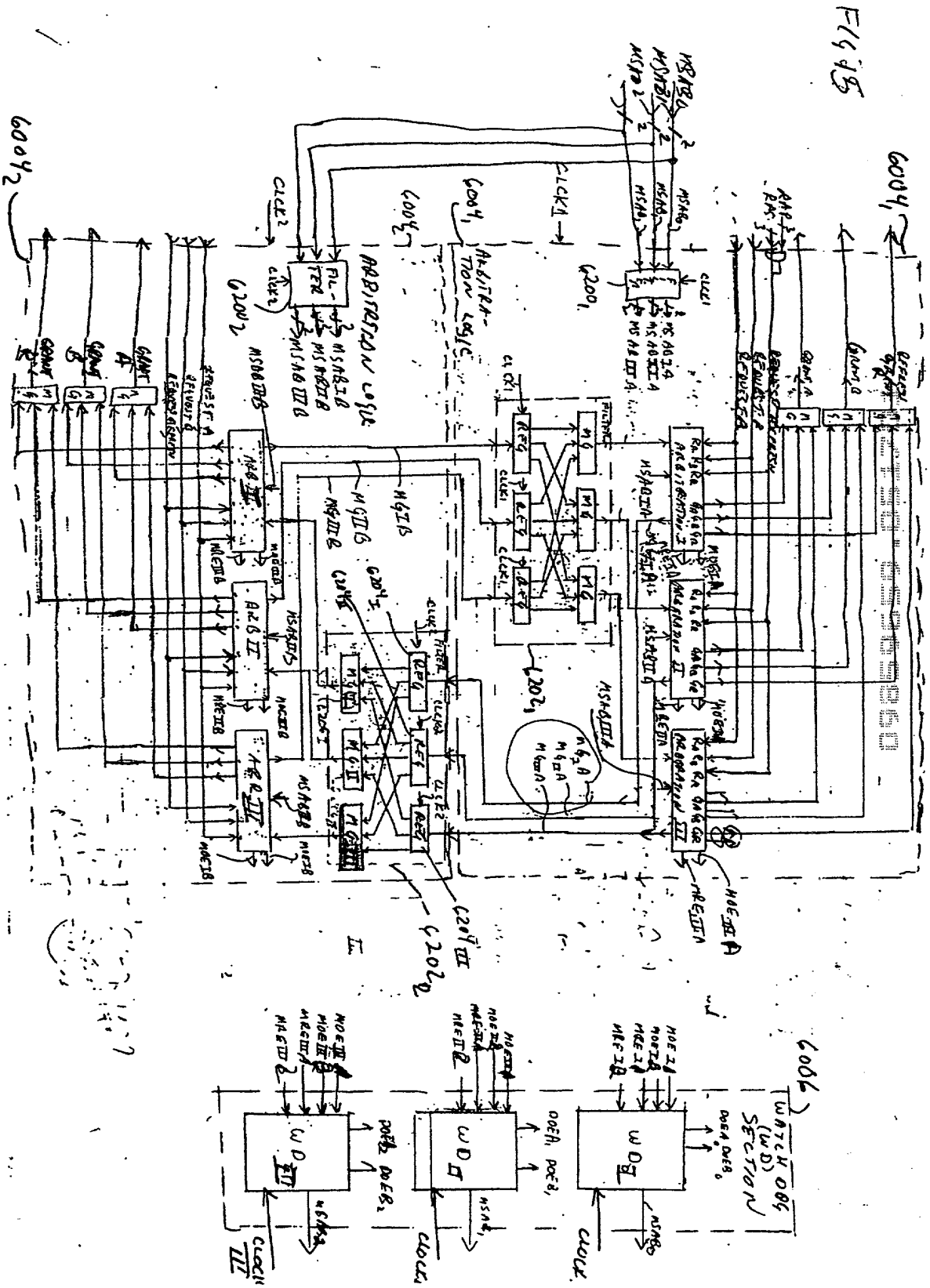

5010
LOGIC SECTION (MEMORY REGION CONTROLLER)
UPPER PORT A CONTROLLER (HIGH)
6002A
UPPER PORT B CONTROLLER
6002B
MEMORY REFRESH SECTION
6002R
ADDR/CONTROL
DATA_WRITE
DATA_READ
PORT_A_SELECT
GRANT_A (GA)
REQUEST_A (RA)
PORT_B_SELECT
GRANT_B (GB)
REQUEST_B (RB)
REFRESH_C
REFRESH_D
PORT_A_SELECT
REFRESH REQUEST (RQ)
REFRESH GRANT (GR)
CLOCK2
PORT_A
PORT_B
5010
5010
MEM-ORY ARRAY
REGION A
ADDRESS
DATA
DOEA
DOEB
6004
ARBITRATION LOGIC
REQUEST A
REQUEST B
REFRESH REQUEST
GRANT A
GRANT B
REFRESH GRANT
MATCH
6005
6006
6007
6008
6009
6010
PORT A SELECT
PORT B SELECT
DATA READ
MODE B
LOGIC SECTION
6004

FIG. 13

Data Storage System Having No-Operation Command
John K. Walton
EMC2-090PUS





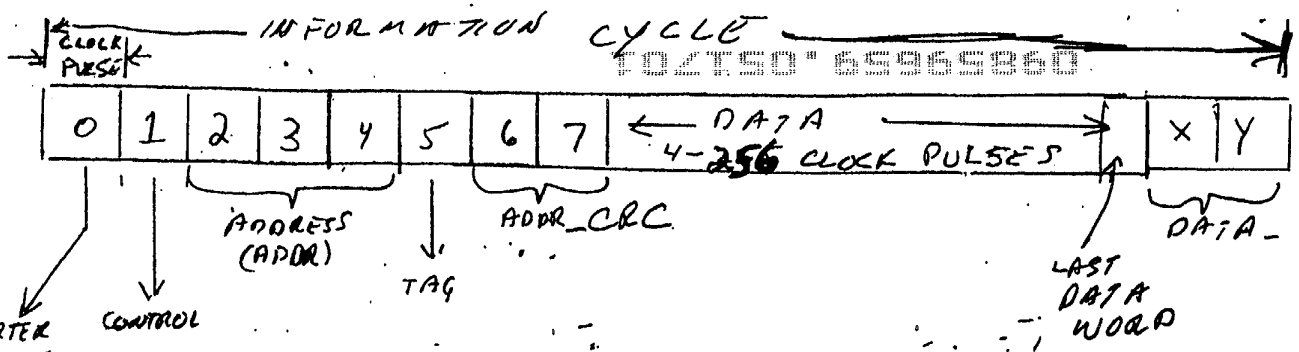


FIG. 16

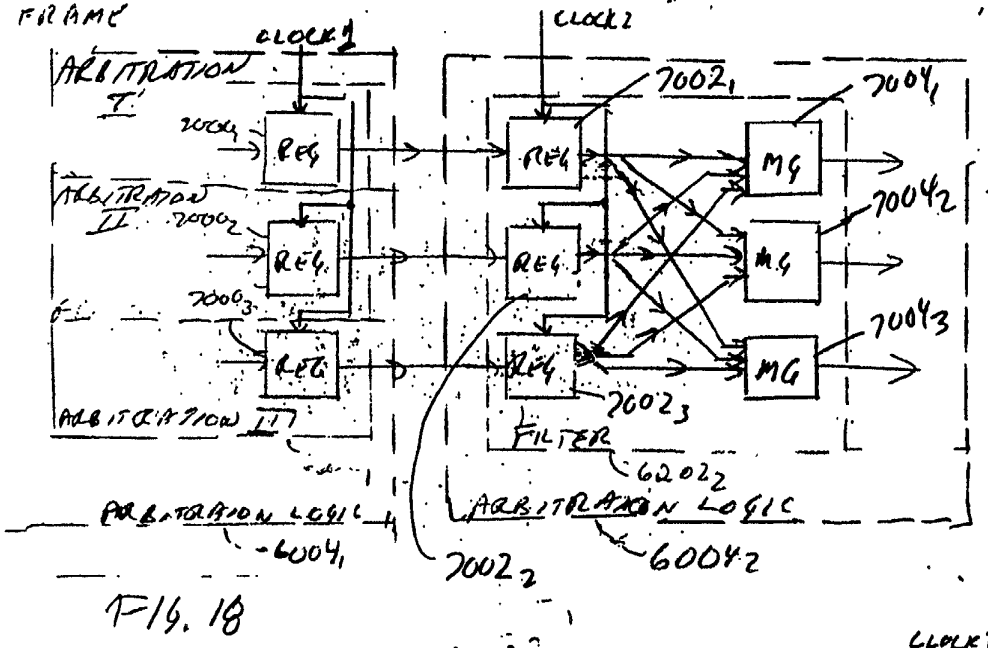


FIG. 18

FIG. 17

MG INPUTS	MG OUTPUT	MG OUTPUT	MG OUTPUT
0 0 0	0	0	0
0 0 1	0	0	0
0 1 0	0	0	0
0 1 1	1	1	1
1 0 0	0	0	0
1 0 1	1	1	1
1 1 0	1	1	1
1 1 1	1	1	1

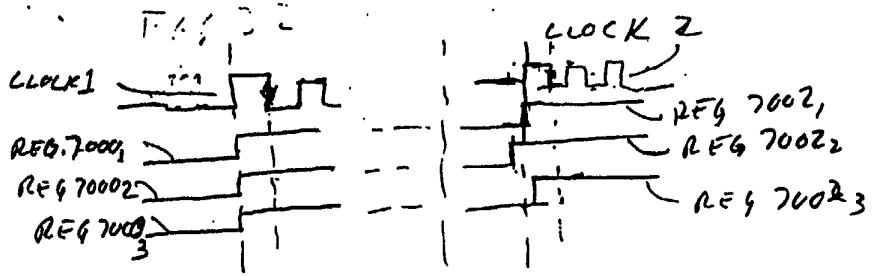
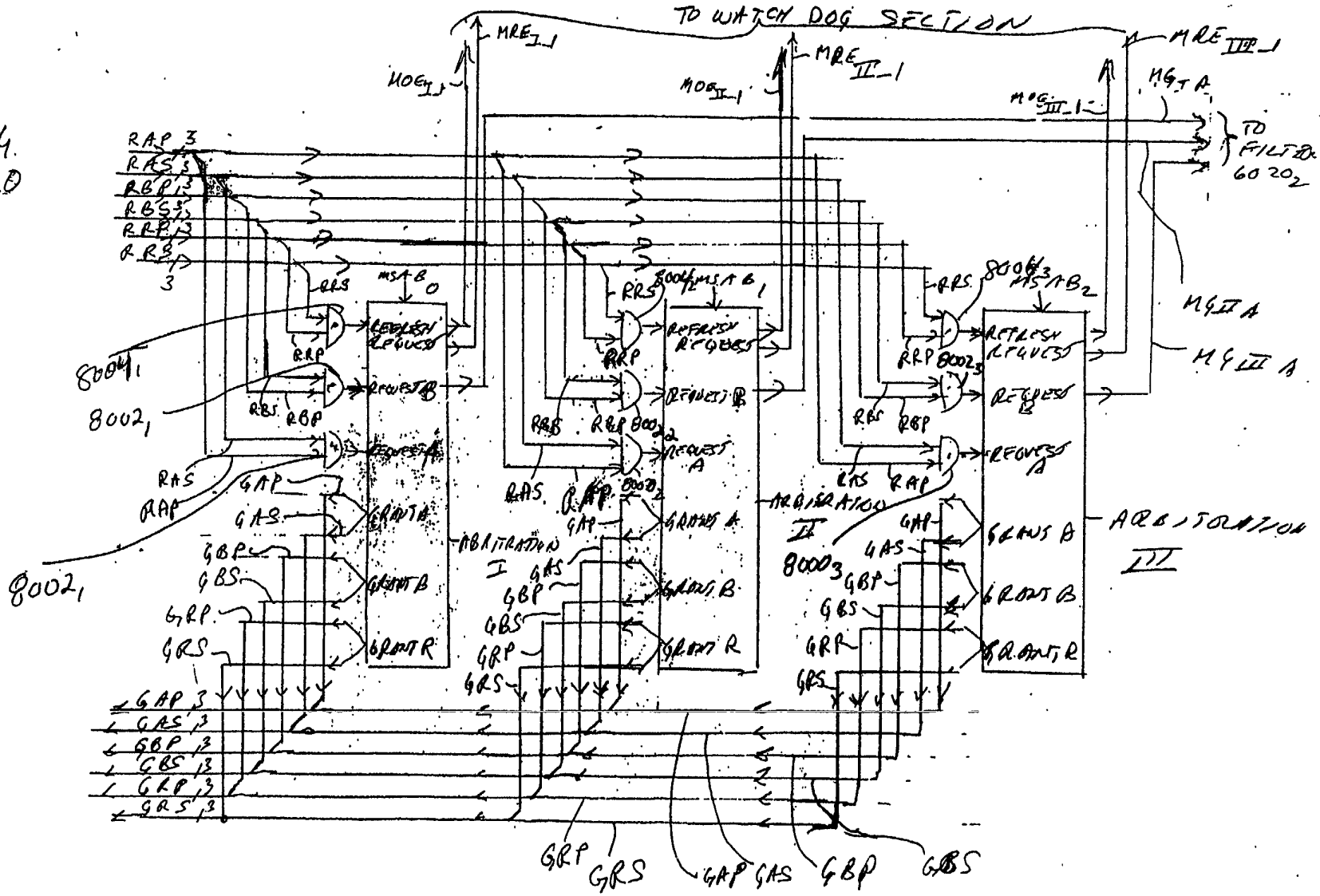


FIG. 19

FIG. 20


TO WATCH DOG SECTION
MRE I-1
MRE II-1
MRE III-1
MG I A
MG II A
MG III A
TO FILTER 6020
ARBITRATION I
ARBITRATION II
ARBITRATION III
RAP 3
RAS 3
RBP 3
RBS 3
RRP 3
RRS 3
GAP 3
GAS 3
GBP 3
GBS 3
GRP 3
GRS 3
8002 1
8002 2
8002 3
GRP
GRS
GAP
GAS
GBP
GBS